# **End-to-End Neural Network Compression via** $\frac{\ell_1}{\ell_2}$ **Regularized Latency Surrogates**

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# Abstract

Neural network (NN) compression via techniques such as pruning, quantization requires setting compression hyperparameters (e.g., number of channels to be pruned, bitwidths for quantization) for each layer either manually or via neural architecture search (NAS) which can be computationally expensive. We address this problem by providing an end-to-end technique that optimizes for model's Floating Point Operations (FLOPs) or for on-device latency via a novel  $\frac{\ell_1}{\ell_2}$  latency surrogate. Our algorithm is versatile and can be used with many popular compression methods including pruning, low-rank factorization, and quantization. Crucially, it is fast and runs in almost the same amount of time as *single model training*; which is a significant training speed-up over standard NAS methods. For BERT compression on GLUE fine-tuning tasks, we achieve 50% reduction in FLOPs with only 1%drop in performance. For compressing MobileNetV3 on ImageNet-1K, we achieve 15% reduction in FLOPs, and 11% reduction in on-device latency without drop in accuracy, while still requiring  $3 \times$  less training compute than SOTA compression techniques. Finally, for transfer learning on smaller datasets, our technique identifies  $1.2 \times -1.4 \times$  cheaper architectures than standard MobileNetV3, EfficientNet suite of architectures at almost the same training cost and accuracy.

# 1 Introduction

Large-scale neural networks consistently provide state-of-the-art performance on complex learning tasks [1, 2, 3]. But they place heavy burden on compute resources such as battery, memory or processor making them hard to deploy on edge devices such as phones, cameras and wearables. Several recent works have designed techniques to compress ML models and make them efficient for inference. However, as detailed below, many of these techniques are hard to use in practice, and often achieve sub-optimal accuracy *vs* inference time trade-offs.

**Hyperparameter search for compression.** Existing works typically rely on one of the following building blocks to design efficient models: unstructured weights sparsity [4, 5], pruning entire neurons or low-rank factorization [6], quantization [7], distillation [8]. Figuring out an optimal way to combine these building blocks (or to figure out hyper-parameters such as amount of sparsity associated with each block) while satisfying a global latency/FLOPs/resource constraint is difficult and involves a combinatorial search. This problem is further exacerbated when multiple building blocks are used for model compression (*e.g.*, simultaneous low rank factorization, sparsity/pruning of weights).

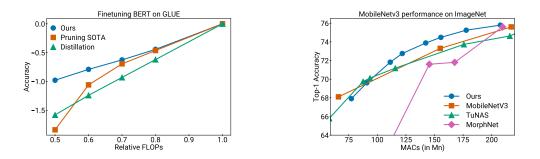


Figure 1: Left plot compares various techniques for BERT compression on GLUE tasks (averaged across tasks). *x*-axis is the relative number of FLOPs as compared to BERT<sub>BASE</sub>. *y*-axis is the relative drop in accuracy from the baseline. Pruning SOTA numbers are taken from [21], while distillation baselines are from [22, 23]. Right plot compares various techniques for MobileNetV3 compression on ImageNet-1K dataset. *MobileNetV3* corresponds to MobileNetV3 models with different width multiplier. *TuNAS, MorphNet* are SOTA techniques for scalable compression. TuNAS takes a blackbox approach to model compression, whereas MorphNet takes a more direct approach by optimizing FLOPs regularized objective.

Over the past few years, there has been a large body of work that addresses the problem of finding hyperparameters for model compression. Existing literature in this space can be broadly categorized as: (a) methods to find hyperparameters of a *specific* building block such as unstructured pruning of weights, (b) Neural Architecture Search (NAS) techniques to find hyperparameters of *any* efficient block. The first set of techniques are naturally limited, but even for the specific blocks considered, their performance on real-world benchmarks is unstable and in fact, can be sub-optimal to the more general approach that we propose in this work (see the left plot in Figure 1). The NAS based techniques are much more generally applicable, but the computational cost of such methods is prohibitive as they typically don't exploit any specific attributes of the popular efficient blocks such as sparsity, pruning.

**Neuron Pruning**: Among the category (a) techniques mentioned above, a prominent line of work has focused on unstructured pruning of weights with non-uniform budget allocation across layers [4, 9, 10, 5]. However, any gain in FLOPs using unstructured pruning is hard to translate to real latency gain as modern hardware – like GPUs, TPUs – are more geared towards dense matrix operations. So it is more fruitful to focus on neuron pruning, which removes entire neurons/channels, and lowrank factorization of weights, which is closely related to neuron pruning. Recent techniques in this line of work add a latency/FLOPs regularizer to the standard cross entropy loss [11, 12] to bias the model towards lower number of neurons. Unfortunately the resulting objective is discrete and difficult to optimize. To alleviate this, existing works have designed continuous surrogates that are more amenable to SGD style optimization. These methods either work in the space of probability distributions over pruned models and optimize the "expected objective" [12, 13, 6] or replace the discontinuous FLOPs regularizer with a continuous surrogate such as  $\ell_1$  norms of the weights of the network [11]. However, the former class of techniques are often unstable, hard to implement in practice, and empirical studies indicate that their performance is similar to that of simple magnitude based pruning [14] (also see left plot of Fig. 1). Furthermore, as we show in this work, the latter class of techniques fail to enforce sparsity in the presence of batch, layer normalization (see Section 3).

**NAS**: Several works in category (b) formulate model compression as a black-box Neural Architecture Search (NAS) problem and rely on state-of-the-art NAS techniques to search for efficient models [15, 16, 17, 18, 19]. These techniques directly take the latency/FLOPs into account and have the potential to identify the optimal per-layer budget allocation for a wide variety of efficient blocks/compression mechanisms. However, these approaches are often computationally expensive as they take a blackbox view of the problem and perform combinatorial search over the space of architectures. Despite recent advances such as TuNAS [18] and DARTS [20], these techniques can be an order of magnitude slower and less accurate than our proposed method (see Fig 1).

**Our Approach**: In this work, we propose an approach that sits right in the middle of the above two mentioned categories. That is, our approach applies to a large class of efficient building blocks – like unstructured sparsity, neuron pruning, quantization – for which we can write the FLOPs computation with a continuous surrogate (see Table 1). Furthermore, to ensure that our FLOPs, latency regularizers work even in the presence of batchnorm, layernorm, we propose a novel surrogate that is based on  $\frac{\ell_1}{\ell_2}$  norm. While our surrogates are continuous, they are non-differentiable. In such cases standard

optimizers such as SGD, Adam can be quite slow to converge [24]. To overcome this, we propose a projection operation on the mask variables, after each SGD step. Our proposed method speeds up the convergence and also outputs *exact sparse solutions* thus eradicating need for post-hoc thresholding, while being simple enough to not increase training time significantly.

We implement our algorithm with multiple building blocks including pruning, low-rank factorization, quantization, and apply it on multiple problems in the domain of image classification and NLP. In particular, we demonstrate the effectiveness of our technique for MobileNetV3 compression on ImageNet (see Fig. 1), where our method can learn an architecture with up to 15% (11%) lower FLOPs (latency) on Pixel 6 mobile phones, without any drop in accuracy. Here our approach is more accurate than MorphNet, a SOTA technique which focus exclusively on neuron-pruning, as well as, TuNAS, a SOTA NAS technique. Furthermore, in terms of training time, our method is  $3 \times$  cheaper than TuNAS. We would like to highlight that MobileNetv3 is a highly optimized architecture found using efficient NAS techniques [25], and our technique is able to compress this architecture further.

One exciting application of our work is that we can apply it to optimize certain "foundational" baseline models for individual fine-tuning tasks. For example, for compression of BERT on GLUE benchmarks, our method achieved 40 - 50% reduction in FLOPs with only 1% drop in accuracy (see Fig 1). Moreover, our technique dominates standard model compression baselines. Similarly for smaller vision classification tasks, our technique compresses MobileNetV3, EfficientNet suite of architectures and identifies  $1.2 \times -1.4 \times$  cheaper architectures without significant loss in accuracy (see Figure 3). We would like to note that all these results are obtained at almost the same cost as that of training a single model for the task. Finally, we also demonstrate the versatility of our method by using it to quantize a CNN on CIFAR-10, and learning the bit-widths (2, 4, 8, 16) for each of its layers. Our technique found a model that is 55% smaller than the baseline float-16 model, while achieving the same accuracy (see Figure 5). While low-bit quantization is not usually exploited by general purpose accelerators to speed up computation, it can still lead to reduction in inference times of large language models such as GPT as these models are memory bandwidth bound [26]. Here is a summary of our contributions:

(1). We provide an end-to-end neural network compression technique that directly optimizes the FLOPs/latency regularized objective during leading to compression during training. Our algorithm can be used with many popular efficient building blocks including pruning, low-rank factorization, quantization, and can optimize for on-device inference latency.

(2). We design a novel  $\frac{\ell_1}{\ell_2}$  regularized surrogate for latency that works even in the presence of batchnorm, layernorm. Our algorithm is fast and runs in the same amount of time as single model training, and doesn't require any post-processing steps.

(3). We demonstrate the performance of our technique on both language and vision tasks. Moreover, for transfer learning settings where the goal is to take a baseline architecture and optimize it for individual tasks, our techniques outperform SOTA techniques in the broad-domain of automated neural compression.

# 2 Related Work

#### 2.1 Neural Architecture Search

Early works on NAS treated the problem as a purely blackbox optimization (BO) problem. These works relied on BO techniques such as random search [27], Gaussian process optimization [17], and zeroth-order gradient descent [15, 16], evolutionary algorithms to optimize the NAS objective and identify a good architecture. Several works have improved upon these algorithms using heuristics such as early stopping [27]. Nonetheless, these techniques are computationally expensive, as evaluating the optimization objective at any point requires training a neural network from scratch. Moreover, due to computational complexity, these techniques perform a very coarse grained search and are not suited for fine-grained search over sparsity or low-rank structures.

Recent works have tried to open the blackbox a bit. In these techniques, the search space is first transformed to the space of probability distributions over architectures. Next, a surrogate model (which takes an architecture as input and tries to output the optimal set of weights for the architecture) is trained to quickly evaluate the optimization objective at any input [18, 20, 28, 29, 12]. While these techniques are fast, they involve joint training of the surrogate model during the search process. This joint training often makes the optimization process unstable [30].

**NAS for Efficient ML.** Several recent works at the intersection of efficient ML and NAS have realized the importance of explicitly accounting for the hardware in the search process [15, 31, 32, 33, 34, 35]. These works incorporate the actual inference time in their search objectives, instead of surrogates such as FLOPs. The inference time maybe estimated using another neural network, or through latency tables for basic arithmetic operations on the target platform [19]. Many of these works rely on greedy, random search heuristics to solve the resulting objective [32, 33]. However, these heuristics either take a lot of time to find the optimal architecture or are not guaranteed to converge to an optimal solution. There are some works that rely on the NAS algorithms described above [15, 31, 18]. However, these techniques face the same issues as previously mentioned.

Hardware, Neural Architecture codesign. Certain hardware level parameters such as tiling configurations of tensors significantly affect the inference time of a model. Recent hardware-aware NAS techniques expose these hardware level parameters to the NAS algorithm and simultaneously search over neural architectures and hardware configurations [35]. These techniques have the potential to achieve better performance than vanilla NAS techniques which do not search over hardware configurations.

#### 2.2 Model Compression

The field of model compression is vast. Here, we focus on techniques that perform training-time compression (as opposed to post-training compression) using the following building blocks: unstructured sparsity, pruning and low-rank factorization. Early works in unstructured sparsity and pruning relied on magnitude, gradient based pruning [4, 36, 14]. Several works have explored more sophisticated scoring metrics for pruning [37, 38, 39, 40, 41]. Other techniques include adding sparsity inducing norms such as  $\ell_0$ ,  $\ell_1$  to the training objective [13, 5]. A number of works have also explored low-rank factorization for model compression [42, 43, 44]. Some of these techniques again rely on sparsity inducing regularizers to induce the low-rank structure [6]. Others rely on SVD based pruning. Some recent works try and optimize FLOPs regularized objective to perform pruning, low-rank factorization [11, 12]. However, as we discussed in the introduction, the resulting optimization techniques are often unstable and difficult to use in practice.

# 3 Method

In this section, we describe our approach for model compression. For simplicity of presentation, we illustrate our technique on feed-forward networks and restrict ourselves to pruning. The ideas here can be extended to other architectures (*e.g.*, 1x1 convolutions in CNNs), and other efficient building blocks (*e.g.*, unstructured sparsity, low-rank factorization, quantization) in a straightforward manner (see Table 1 for details). Consider the following problem: we are given a pre-trained feed forward neural network (FFN)  $f^*(x) = \sigma(W_D^* \sigma(W_{D-1}^* \sigma(\dots \sigma(W_1^* x))))$ , where  $W_i^* \in \mathbb{R}^{d_{i+1} \times d_i}$  for all  $i \in [D]$ , and a dataset  $\{(x_i, y_i)\}_{i=1}^n$ . Our goal is to compress  $f^*$  while simultaneously performing well on the learning task. This problem can be formulated as the following optimization problem

$$\min_{\mathcal{W}} \frac{1}{n} \sum_{i=1}^{n} \ell(x_i, y_i; \mathcal{W}) + \lambda \times \text{Latency}(\mathcal{W}).$$
(1)

Here  $\mathcal{W} = \{W_i\}_{i=1}^D$ , with  $W_i \in \mathbb{R}^{d'_{i+1} \times d'_i}$  being the weight matrix at layer  $i, \lambda$  is the regularization parameter which trades-off latency with accuracy and  $\ell$  is the supervised loss.<sup>1</sup>. Directly optimizing the above objective is intractable because Latency( $\mathcal{W}$ ) is a discrete function of the dimensions of weight matrices, and is hardware specific.

We now present our technique for solving Equation (1). To begin with, we substitute Latency(W) with FLOPs(W)<sup>2</sup>. Later, we extend it to actual latency. The objective in this case is given by

$$\min_{\mathcal{W}} \frac{1}{n} \sum_{i=1}^{n} \ell(x_i, y_i; \mathcal{W}) + \lambda \sum_{i=1}^{D} d'_i d'_{i+1}.$$
 (2)

<sup>&</sup>lt;sup>1</sup>In this objective, we search over  $d'_i$  such that  $d'_i \leq d_i$ 

<sup>&</sup>lt;sup>2</sup>FLOPs is also a discrete function of dimensions of  $W_i$ , and the resulting optimization problem is still intractable

To solve this objective, we associate masks with each neuron in the network. In particular, we parameterize the weight matrix in the  $i^{th}$  layer as  $W_i \times \text{diag}(\alpha_i)$ . Here  $\alpha_i \in \{0, 1\}^{d_i}$  are the mask variables of layer *i*. If  $\alpha_{i,j}$  is set to 0, then the  $j^{th}$  neuron in the  $(i-1)^{th}$  layer will be pruned. The FLOPs regularizer can now be written in terms of masks as  $\sum_{i=1}^{D} ||\alpha_i||_0 ||\alpha_{i+1}||_0$ , where  $\alpha_{D+1}$  is the static vector of all 1's. The resulting objective though is not continuous. To make it continuous and amenable to gradient based optimization, one class of techniques place a Bernoulli distribution Bern $(p_{i,j})$  over each of the masks  $\alpha_{i,j}$  and solve the following smoothed objective [12, 13, 6]

$$\min_{\mathcal{W},p} \mathbb{E}\left[\frac{1}{n}\sum_{i=1}^{n}\ell(x_i, y_i; p, \mathcal{W}) + \lambda \sum_{i=1}^{D} \|\alpha_i\|_0 \|\alpha_{i+1}\|_0\right]$$

The expectation above is taken w.r.t the random masks  $\alpha_i$ 's. It is easy to see that the above objective is equivalent to Equation (2), and is consequently as hard as solving the latter. In fact, the above problem can be shown to be NP-hard using the observation that sparse linear regression is a special case of it [45]. Furthermore, the discrete nature of  $\alpha_i$ 's makes the optimization process unstable [13]. To overcome this, [12, 13, 6] rely on a heuristic which involves relaxing Bernoulli distribution to a continuous distribution such as LogisticSigmoid. However, the main drawback of the resulting algorithm is that it is hard to implement in practice and requires very careful annealing of the parameters of LogisticSigmoid distribution. Another drawback of this class of techniques is that their performance is not well understood theoretically, even for simple and fundamental problems such as sparse linear regression.

Another approach to convert the discrete objective in Equation (2) into a continuous function is to replace the  $\ell_0$  norm on  $\alpha_i$ 's with  $\ell_1$  norm

$$\min_{\mathcal{W},\alpha_i \in \mathbb{R}^{d_i}} \frac{1}{n} \sum_{i=1}^n \ell(x_i, y_i; \alpha, \mathcal{W}) + \lambda \sum_{i=1}^D \|\alpha_i\|_1 \|\alpha_{i+1}\|_1.$$
(3)

This approach is much more attractive than the previous approach as it is known to recover the optimal sparse solutions for a variety of statistical problems including sparse linear regression, low-rank matrix completion [46, 47]. Furthermore, it is much simpler to implement in practice, with numerous algorithms being proposed for fast convergence to the stationary points of the objective [24, 48]. Consequently, recent SOTA compression techniques relied on  $\ell_1$  norm surrogates to compute the FLOPs regularizer [11]. A major drawback of  $\ell_1$  norm though is that it does not promote sparsity in the presence of batch normalization and layer normalization [49, 50]. To see this, consider the following 1-hidden layer network:  $\sigma(BN(W_2 \operatorname{diag}(\alpha_2)\sigma(BN(W_1 \operatorname{diag}(\alpha_1)x)))))$ . One can scale down all entries of  $\alpha_1$  and scale up the weights  $W_1$  without affecting the output of the network. Doing this reduces the objective value in Equation (3), but doesn't induce any sparsity in the network. In practice, we in fact notice this behaviour during optimization of Equation (3), which leads to suboptimal solutions (see Section 3.2). Note that adding  $\ell_2$  penalty on the weights (*i.e.*, weight decay) doesn't mitigate this issue as any scaling of  $\alpha$ 's can be absorbed by the batch norm parameters without changing the output of the network.

# 3.1 Inducing sparsity through $\frac{\ell_1}{\ell_2}$ regularizer

We now introduce our approach for making the objective in Equation (2) continuous. We replace  $\ell_0$  norm over masks ( $\|\alpha_i\|_0$ ) with  $\frac{\ell_1}{\ell_2}$  penalty ( $\sqrt{d_i}\|\alpha_i\|_1/\|\alpha_i\|_2$ ) and solve the following optimization problem

$$\min_{\mathcal{W},\alpha_i \in \mathbb{R}^{d_i}} \frac{1}{n} \sum_{i=1}^n \ell(x_i, y_i; \alpha, \mathcal{W}) + \lambda \sum_{i=1}^D \frac{\sqrt{d_i} \|\alpha_i\|_1}{\|\alpha_i\|_2} \frac{\sqrt{d_{i+1}} \|\alpha_{i+1}\|_1}{\|\alpha_{i+1}\|_2}.$$
(4)

The  $\sqrt{d_i}$  term in the numerator normalizes the penalty to lie between  $[0, d_i]$ . When  $\alpha_i$ 's are all 1's, the regularizer evaluates to FLOPs. Observe that this regularizer is invariant to scaling of  $\alpha$ 's. Consequently, the value of the regularizer cannot simply be reduced by scaling down  $\alpha_i$ 's. In our experiments in sec 3.2 and Appendix C.2, we show that this handles batch, layer normalizations better than  $\ell_1$  regularizer. Several works have studied this regularizer in the context of sparse linear regression and showed that is recovers the underlying sparse signal under mild conditions on the

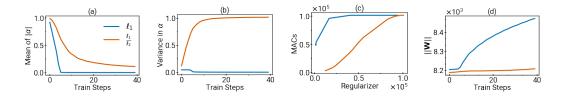


Figure 2: Comparison of  $\ell_1$ ,  $\frac{\ell_1}{\ell_2}$  induced FLOPs regularizer for pruning on FashionMNIST: Figures (a) and (b) depict the evolution of the statistics of the mask variables ( $\alpha$ ) as training progresses. Figure (c) shows the relation between the actual FLOPs of the model and the value of the proxy computed by Equations 3, 4. Figure (d) shows the evolution of the Frobenius norm of the weight matrix.

data [51, 52, 53]. [54] used a similar  $\frac{\ell_1}{\ell_2}$  regularizer for network pruning, but their technique doesn't optimize latency or FLOPs, and relies on post-training thresholding to get sparsity.

For certain technical reasons described later, we add a positivity constraint on  $\alpha_i$ 's and solve the following objective

$$\min_{\mathcal{W},\alpha_i \in \mathbb{R}^{d_i}_+} \frac{1}{n} \sum_{i=1}^n \ell(x_i, y_i; \alpha, \mathcal{W}) + \lambda \sum_{i=1}^D \frac{\sqrt{d_i} \sum_{j=1}^{d_i} \alpha_{i,j}}{\|\alpha_i\|_2} \frac{\sqrt{d_{i+1}} \sum_{j=1}^{d_{i+1}} \alpha_{i+1,j}}{\|\alpha_{i+1}\|_2}.$$
 (5)

Note that we consider  $\alpha \in \mathbb{R}^{d_i}_+$  rather that discrete or bounded values. We would like to highlight that this change doesn't reduce the representational power of our model. It is mainly done for computational reasons. In the sequel, we use the shorthand  $\|\alpha_i\|_{1p}$  (*p* for positive) to denote  $\sum_{j=1}^{d_i} \alpha_{i,j}$ .

**Importance of positivity constraints.** The objective in Equation (4) is continuous, but not smooth. For such losses, standard optimization techniques such as SGD, Adam are slow to converge to stationary points [55]. Furthermore, these algorithms don't output exact sparse solutions. This forces additional post-processing steps to be introduced into the compression pipeline. For example, [11, 54] rely on Adam optimizer and add a pruning step at the end, where masks that are close to 0 are pruned away. This is quite cumbersome in practice as one needs to choose appropriate thresholds for pruning, which introduces an additional tunable hyper-parameter, and needs re-training after pruning. To overcome this, we add a positivity constraint to the mask variables and modify the objective to Equation (5). This makes the regularizer smooth (except at all 0's vector), and easy to optimize using SGD, Adam. After each SGD/Adam update, we simply project the masks back to the space of positive real numbers. The overall update looks as follows

$$\mathcal{W} \leftarrow \mathcal{W} - \eta \nabla_{\mathcal{W}}(\mathcal{L}(\alpha, \mathcal{W}) + \lambda \mathcal{R}(\alpha)), \quad \alpha \leftarrow \max(0, \alpha - \eta \nabla_{\alpha}(\mathcal{L}(\alpha, \mathcal{W}) + \lambda \mathcal{R}(\alpha))).$$

Here  $\mathcal{L}(\alpha, W)$  is the empirical risk and  $\mathcal{R}(\alpha)$  is the regularizer. Notice, the only additional step compared to traditional optimization, is the clipping of  $\alpha$ 's. In our ablation studies in Sec 3.2 and App C.2, we validate the importance of this projection step, together with  $\frac{\ell_1}{\ell_2}$  norm, in encouraging sparse solutions.

#### 3.2 Verification of design choices

To empirically demonstrate the drawbacks of using  $\ell_1$  penalty for model compression, we perform experiments on the FashionMNIST dataset with a single hidden layer fully connected network which has a batch norm layer after the first linear layer. We prune out the input to the network using a mask  $\alpha$  on the input. We compare the performance of networks compressed using FLOPs regularizer induced by  $\ell_1$  and  $\frac{\ell_1}{\ell_2}$  norms. We use SGD for optimization of both the objectives. Furthermore, we pre-train the network using standard CE loss, and initialize  $\alpha = 1$ . We track the variance of the absolute values of the entries of  $\alpha$ , i.e.  $\frac{\sum_{i=1}^{d} (|\alpha_i| - \mu_{\alpha})^2}{d}$ , where  $\mu_{\alpha} = \frac{\sum_{i=1}^{d} |\alpha_i|}{d}$ . We also track the mean  $\mu_{\alpha}$  of the absolute values of the entries of  $\alpha$ . Finally, we plot out the curve between FLOPs and the considered norm of  $\alpha$  (*i.e.*,  $\ell_1$ ,  $\frac{\ell_1}{\ell_2}$ ). Figure 2 presents the results from these experiments. We can see that the  $\ell_1$  objective is mis-aligned with the actual value of FLOPs, while the regularizer computed using  $\frac{\ell_1}{\ell_2}$  is a better proxy. We also find that the mean and variance of  $\alpha'$ 's sharply decreases when  $\ell_1$ induced FLOPs regularizer is used for compression. This indicates that all entries of  $\alpha$  are uniformly

Table 1: Table describing regularizers used by our technique for various efficient building blocks (refer to Appendix for details on quantization). One can easily design regularizers for searching over a combination of building blocks. For example, last row presents regularizer for low-rank + pruning, which we use in our large-scale experiments.

Efficient Building Block	Parameterization of $W_i$	<b>FLOPs</b> $(i^{th} layer)$	$\begin{array}{c} \textbf{Regularizer (FLOPs surrogate)} \\ (i^{th} \text{ layer}) \end{array}$
Pruning	$W_i  imes \operatorname{diag}(\alpha_i)$	$\ \alpha_i\ _0\ \alpha_{i+1}\ _0$	$\frac{\sqrt{d_i} \ \alpha_i\ _{1p}}{\ \alpha_i\ _2} \frac{\sqrt{d_{i+1}} \ \alpha_{i+1}\ _{1p}}{\ \alpha_{i+1}\ _2}$
Unstructured Sparsity	$W_i \odot \alpha_i, \text{ where } \alpha_i \in \mathbb{R}^{d_{i+1} \times d_i}_{\text{o}},$ $\odot \text{ is the elementwise multiplication operator}$	$\ \operatorname{Vec}(lpha_i)\ _0$	$\frac{\sqrt{d_i d_{i+1}} \  \operatorname{Vec}(\alpha_i) \ _{1p}}{\  \operatorname{Vec}(\alpha_i) \ _2}$
Low-rank Factorization	$U_i \operatorname{diag}(\beta_i) V_i,$ where $U_i \in \mathbb{R}^{d_{i+1} \times d_{i,*}},$ $d_{i,*} = \min\{d_i, d_{i+1}\}$	$(d_i + d_{i+1}) \  \beta_i \ _0$	$(d_i + d_{i+1}) \frac{\sqrt{d_{i,*}} \ \beta_i\ _{1p}}{\ \beta_i\ _2}$
Quantization $(1, 2, 4 \text{ bit quantization})$	$ \begin{array}{l} W_{i,1} + \alpha_{i,2}(\Delta_{i,2} + \alpha_{i,4}(\Delta_{i,4})), \\ \text{where } \alpha_{i,2}, \alpha_{i,4} \in [0,1], \text{ are} \\ \text{mask variables, } W_{i,b} \text{ is the} \\ b\text{-bit quantization of } W_{i,} \\ \Delta_{i,2} = W_{i,2} - W_{i,1}, \\ \Delta_{i,4} = W_{i,4} - W_{i,2} \end{array} $	$ \begin{aligned} \ (1-\alpha_{i,2})\ _0 d_i d_{i+1} + \\ 2\ \alpha_{i,2}(1-\alpha_{i,4})\ _0 d_i d_{i+1} + \\ 4\ \alpha_{i,2}\alpha_{i,4}\ _0 d_i d_{i+1} \end{aligned} $	$\begin{array}{l} \frac{\ell_{1}}{\ell_{2}} \text{ norm over} \\ \text{the vector } \left[ \left( 1 - \alpha_{i,2} \right), \\ 2\alpha_{i,2} \left( 1 - \alpha_{i,4} \right), 4\alpha_{i,2}\alpha_{i,4} \right] \\ \times d_{i}d_{i+1} \end{array}$
Pruning + Low-rank Factorization	$U_{i} \text{diag}(\beta_{i}) V_{i} \text{diag}(\alpha_{i}),$ where $U_{i} \in \mathbb{R}^{d_{i+1} \times d_{i,*}},$ $d_{i,*} = \min\{d_{i}, d_{i+1}\}$	$(\ \alpha_i\ _0 + \ \alpha_{i+1}\ _0)\ \beta_i\ _0$	$ \begin{pmatrix} \frac{\sqrt{d_i} \ \alpha_i\ _{1p}}{\ \alpha_i\ _2} + \frac{\sqrt{d_{i+1}} \ \alpha_{i+1}\ _{1p}}{\ \alpha_{i+1}\ _2} \\ \times \frac{\sqrt{d_{i,*}} \ \beta_i\ _{1p}}{\ \beta_i\ _2} \end{pmatrix} $

scaled down to a small, non-zero value, reducing the value of the regularizer, while not providing any sparsity. As seen from the figure,  $\frac{\ell_1}{\ell_2}$  does not suffer from this drawback. Finally, we note that the frobenius norm of the weight matrix W increases when  $\ell_1$  regularization is used on  $\alpha$ , suggesting that the network is simply scaling down  $\alpha$ 's and scaling up the weights to evade the regularizer.

#### 3.3 Hardware aware model compression

In this section, we extend the FLOPs regularizer to take the latency on the target hardware into account. The resulting regularizer is especially useful for performing hardware aware network compression. Our key observation is that the inference on a neural network can be broken down into a series of matrix multiplication operations. For example, inference on a depth D FFN involves D matrix-vector multiplications, which take-up majority of the time. So, getting a good estimate of the inference time of the overall network boils down to having a good estimate of the latency of matrix-vector multiplication. To this end, we rely on lookup tables. Before the start of the pruning phase, we construct a 2-dimensional lookup-table T whose  $(d_1, d_2)^{th}$  entry is the on-device latency of multiplying a matrix of size  $d_1 \times d_2$  with a vector of size  $d_2$ . Such a table is easy to construct, given access to the target device. Next, to incorporate the look-up table T into our pruning algorithm, we convert it into a continuous function by performing linear interpolation on the entries in the table [56]. To be precise, for any  $(x, y) \in [d_1, d_1 + 1] \times [d_2, d_2 + 1]$ , where  $d_1, d_2 \in \mathbb{N} \cup \{0\}$ , we define T(x, y) as:  $T(x, y) = t_1 + (t_2 - t_1)(y - d_2)$ , where  $t_1 = T(d_1, d_2) + (T(d_1 + 1, d_2) - T(d_1, d_2))(x - d_1)$ , and  $t_2 = T(d_1, d_2 + 1) + (T(d_1 + 1, d_2 + 1) - T(d_1, d_2 + 1))(x - d_1)$ . Note that in contrast to black-box NAS techniques like [19] which search over a discrete space of number of filters for each block, our approach needs the latency surrogate to be differentiable, and hence we need interpolated latency tables. See the appendix for details on how we construct the tables.

We use this interpolated lookup table to construct our latency regularizer as follows

$$\sum_{i=1}^{D} T\left(\frac{\sqrt{d_i} \|\alpha_i\|_{1p}}{\|\alpha_i\|_2}, \frac{\sqrt{d_{i+1}} \|\alpha_{i+1}\|_{1p}}{\|\alpha_{i+1}\|_2}\right).$$
(6)

In the above expression, our differentiable surrogate for  $\|\alpha_i\|_0$  (*i.e.*,  $\sqrt{d_i}\|\alpha_i\|_{1p}/\|\alpha_i\|_2$ ), is used to index the lookup table. We note that  $\frac{\ell_1}{\ell_2}$  norm is very crucial for this technique to be successful. This is because  $\frac{\sqrt{d_i}\|\alpha_i\|_{1p}}{\|\alpha_i\|_2}$  is normalized and always lies between  $[0, d_i]$ . In contrast, using  $\ell_1$  norm surrogate in the regularizer gives us  $T(\|\alpha_i\|_1, \|\alpha_{i+1}\|_1)$ . Scaling  $\alpha_i$  by a constant can drastically change this regularizer, and makes the optimization unstable.

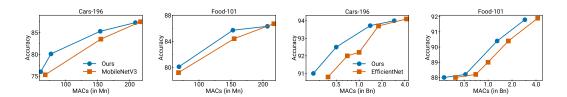


Figure 3: Accuracy-FLOPs trade-off on transfer learning tasks: Figures (a) and (b) depict the the fine-tuning performance of models found by our method while compressing MobileNetv3Large and baseline MobileNetV3 on Cars-196 and Food-101 datasets. Figures (c) and (d) show the performance on the EfficientNet family of architectures, where baselines are EfficientNetB0-B4, while our method compresses EfficientNet B4 and B2.

# 4 Experiments

In this section, we apply our framework to large scale pre-training and transfer learning tasks on standard language and vision benchmarks. To demonstrate the versatility of our technique, we perform experiments on multiple model families (MobileNet, EfficientNet [2], BERT), and multiple building blocks (pruning, low-rank factorization, quantization). We also present a case study using the actual on-device latency instead of FLOPs. See Appendix C.2 for other ablation studies.

#### 4.1 ImageNet Pre-training

We begin by comparing the performance of our technique with baselines on MobileNetV3 compression, for ImageNet classification. We rely on low-rank factorization + pruning for the compression. The results from this experiment are presented in Figure 1. By varying the strength of our regularization, we obtain models with different MACs and accuracies. We find that models produced by our method significantly outperform MobileNetV3 and TuNAS in the high and mid-MACs regime. In particular, for the same accuracy as MobileNetV3Large, our approach finds a model with 15% fewer MACs. In comparison with TuNAS, we achieve 30% reduction in MACs at the same level of accuracy. We however find that our model is at par with MobileNetV3Small in the low MACs regime, indicating that the former is already well-tuned for this task. In terms of compute needed for training, TuNAS is the most expensive among all the techniques we tried; it took 2 days to train with our hardware setup. In contrast, our method took 13 hours  $(3 - 4 \times faster than TuNAS)$ , and MorphNet took 10 hours.

#### 4.2 Transfer Learning

A common paradigm in deploying machine learning models today is to first pre-train them on a large scale dataset such as ImageNet, and then fine-tune them for the desired target task. However, deploying large models is not feasible on edge devices. Our technique provides a light-weight modification to the standard fine-tuning procedure by producing a compressed model with comparable transfer learning performance on the specific task. We demonstrate this on vision and language tasks.

**Vision tasks.** We consider the task of fine-tuning an ImageNet pre-trained model for a smaller dataset. We consider Cars196 [57] and Food101 [58] as the target datasets, and compare against the MobileNetV3 and EfficientNet families of models. We use ImageNet pre-trained models for initialization. We plot the FLOP-accuracy curves in Fig 3. We compress MobileNetv3Large and EfficientNet-B4 and EfficientNet-B2 architectures while transferring them to the target target task. We find that our method consistently improves over baseline architectures across various FLOPs regimes. This is because our technique is able to adaptively prune the model based on the difficulty of the classification task. On both the tasks, we see 1% accuracy gains over MobileNetV3 small. The accuracy gains on both datasets. On EfficientNet, we see upto 40% reduction in FLOPs without any drop in accuracy on Food101, and around 20% reduction in FLOPs on the Cars196 dataset for the largest models (B4). We also see around 30% FLOP reduction while maintaining the transfer learning performance of the B1 and B0 variants. This demonstrates that our learnt models can scale better than the heuristic scaling described in [2]. See the appendix for additional results.

**Fine-tuning BERT on GLUE.** We consider 5 datasets of the GLUE benchmark [59] that are commonly used in the literature, and fine-tune a pre-trained BERT-Base model with our FLOPs regularizer. We re-parameterize the weight matrices of the feed forward network of each transformer block with our low-rank+sparse parameterization. We compare our approach against model pruning,

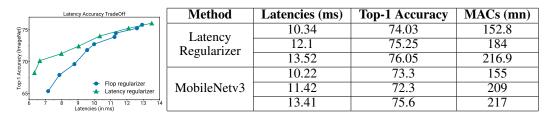


Figure 4: Left plot shows the accuracy-latency curves of models obtained using FLOPs, latency regularizers. Right table compares the performance of our latency regularized models with MobileNetV3 baseline.

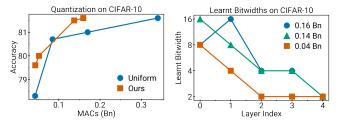


Figure 5: **Quantization on CIFAR-10**: Figure (a) compares the performance of our technique for dynamic quantization against fixed-bit quantization for a 4 layer CNN on CIFAR-10. The baselines have weights quantized to 2,4,8, 16 bits. Fig (b) depicts the learnt bitwidths for different layers of the models found by our technique, with the labels denoting the number of MACs (in Bn) of the models.

where SOTA numbers are taken from Fig. 6 of [21], reporting the maximum accuracy among [60, 61, 62, 63, 64, 65]. We also report the performance of widely-used distillation based baselines [22, 23]. Figure 1 presents the average performance on the 5 datasets, and Figure 6 in appendix presents the individual performance. In both these figures, we plot the relative FLOPs of the compressed model w.r.t BERT-base against the drop in accuracy w.r.t BERT-base (similar to [21]). We find that on 4 of the 5 datasets considered, our technique provides a higher accuracy for the same number of FLOPs, indicating the efficacy of our method. On MRPC, a dataset with very few samples, our method is worse off on higher FLOPs, but outperforms the baselines in the low FLOP regime.

#### 4.3 Additional Experiments

Using the latency regularizer. In Eq 6, we propose a latency surrogate for optimizing the actual on-device inference latency. In this section, we provide empirical evidence of the effectiveness of this approach for MobileNetv3 on Pixel 6. We compare the accuracy-latency curves of models produced using FLOPs, latency regularizers (see Fig 4). Observe that using the latency regularizer leads to models with smaller latencies and consequently better latency-accuracy tradeoff compared to using the FLOP regularizer. We also find these models to have better performance than MobileNetV3 (0.5 - 2% improvement in accuracy for similar latency), despite MobileNetv3 being hand-crafted for faster inference on mobile devices.

**Quantization.** In this set of experiments, we consider CIFAR-10 classification and compress a 3 layer CNN using quantization. We use the quantization formulation presented in Table 1 and search over  $\{2, 4, 8, 16\}$  bit quantizations for each layer. We compare with a baseline which uses the same level of quantization at each layer. Fig 5 presents the results from this experiments. The details of the implementation can be found in the appendix. We find that our technique compresses the model size by almost 55% without drop in accuracy (as compared to a model with 16-bit weights). Our technique also outputs a model which is 1.4% more accurate than a 2-bit quantized model with only 4% more FLOPs. In the plot on the right in Fig 5, we visualize the learned bit-widths of our models. We find that later layers are assigned a smaller bit width, indicating the importance of learning expressive filters early in the network. The different models in our plots were found by varying the the value of the regularizer coefficient, and hence no combinatorial search over bit-widths is required.

# 5 Conclusion and Future Work

In this work, we presented an end-to-end technique for neural network compression. Our approach applies to a wide variety of efficient blocks including pruning, unstructured sparsity, quantization. At

the core of our algorithm is a novel surrogate for FLOPs, latency that relies on  $\frac{\ell_1}{\ell_2}$  norms, and works with batchnorm, layernorm. Our algorithm is computationally efficient and runs in same amount of time as needed for training a single model. We demonstrated the efficacy of our approach on various pre-training and transfer learning tasks on standard language and vision benchmarks. As a future work, it will useful to incorporate more efficient building blocks such as block diagonal matrices into our framework. Another interesting direction would be to make our technique more hardware aware by incorporating hardware level parameters such as tiling into our search process.

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# Appendix

#### A **Re-parameterization for Quantization**

In this section, we present the parameterization of  $W_i$  for quantization. Similar to the main paper, we consider a FFN. For each layer of the network, we would like to search over  $\{1, 2, 4...B\}$  bit quantizations of its weights<sup>3</sup>. Let  $W_i$  be the weight matrix of layer *i*. Let  $clip(W_i; r_{i,l}, r_{i,u})$  be the weight matrix restricted to  $[r_{i,l}, r_{i,u}]$ 

$$\operatorname{clip}(W_i; r_{i,l}, r_{i,u}) = r_{i,u} - \operatorname{ReLU}(r_{i,u} - r_{i,l} - \operatorname{ReLU}(W_i - r_{i,l})).$$

When clear from the context, we use the short hand notation  $\operatorname{clip}(W_i)$  to denote  $\operatorname{clip}(W_i; r_{i,l}, r_{i,u})$ . Let  $W_{i,b}$  to be the *b*-bit quantization of  $W_i$ , and let  $r_{i,l}^{(b)}, r_{i,u}^{(b)}$  be the range parameters associated with  $W_{i,b}$ . W<sub>i,b</sub> is obtained by uniformly gridding the range  $(r_{i,u}^{(b)} - r_{i,l}^{(b)})$  into 2<sup>b</sup> points and assigning each element of  $W_i$  to its nearest grid point

$$W_{i,b} = r_{i,l}^{(b)} + \frac{r_{i,u}^{(b)} - r_{i,l}^{(b)}}{2^b - 1} \left\lfloor \frac{\operatorname{clip}(W_i) - r_{i,l}^{(b)}}{(r_{i,u}^{(b)} - r_{i,l}^{(b)})/(2^b - 1)} \right\rceil.$$

Here  $\lfloor \cdot \rceil$  denotes the round-to-nearest-integer function. To choose between  $W_{i,1}, W_{i,2} \dots W_{i,B}$ , we introduce binary mask variables  $\alpha_{i,1}, \alpha_{i,2} \dots \alpha_{i,B}$ . This leads us to the following parameterization of  $W_i$ 

$$\alpha_{i,1} \left( W_{i,1} + \alpha_{i,2} \left( W_{i,2} - W_{i,1} + \alpha_{i,4} \left( W_{i,4} - W_{i,2} + \alpha_{i,8} \left( \dots \right) \right) \right) \right)$$
(7)

 $\alpha_{i,b} = 0$  implies the weights can be parameterized with fewer than b bits. Observe that the above expression can be rewritten as

$$\alpha_{i,1}(1-\alpha_{i,2})W_{i,1}+\alpha_{i,1}\alpha_{i,2}(1-\alpha_{i,4})W_{i,2}+\alpha_{i,1}\alpha_{i,2}\alpha_{i,4}(1-\alpha_{i,8})W_{i,4}\dots$$

The FLOPs needed to compute the output of this layer is given by

$$[\|\alpha_{i,1}(1-\alpha_{i,2})\|_{0} + 2\|\alpha_{i,1}\alpha_{i,2}(1-\alpha_{i,4})\|_{0} + 4\|\alpha_{i,1}\alpha_{i,2}\alpha_{i,4}(1-\alpha_{i,8})\|_{0} + \dots] d_{i}d_{i+1}$$

Since searching for binary masks is computationally intractable, we make them continuous; that is, we let  $\alpha_{i,b} \in [0,1], \forall b \in \{1, 2, 4, ..., B\}$ . We consider a continuous FLOPs surrogate which is obtained by computing  $\ell_1/\ell_2$  norm of

$$[\alpha_{i,1}(1-\alpha_{i,2}), 2\alpha_{i,1}\alpha_{i,2}(1-\alpha_{i,4}), 4\alpha_{i,1}\alpha_{i,2}\alpha_{i,4}(1-\alpha_{i,8})\dots].$$

This leads us the following regularizer

$$\frac{\alpha_{i,1}(1-\alpha_{i,2})+2\alpha_{i,1}\alpha_{i,2}(1-\alpha_{i,4})+4\alpha_{i,1}\alpha_{i,2}\alpha_{i,4}(1-\alpha_{i,8})\dots}{\sqrt{(\alpha_{i,1}(1-\alpha_{i,2}))^2+(2\alpha_{i,1}\alpha_{i,2}(1-\alpha_{i,4}))^2+(4\alpha_{i,1}\alpha_{i,2}\alpha_{i,4}(1-\alpha_{i,8}))^2}\dots}d_i d_{i+1}.$$

**Remark 1.** Our  $\ell_1/\ell_2$  regularizer typically outputs  $\alpha_i$ 's that are close to 0/1. In many cases these in fact turn out to be exactly equal to 0/1. In the scenario where they are not equal to 0, 1, we project  $\alpha_{i,b}$ 's to  $\{0,1\}$ . This makes sure we have quantized weights.

**Remark 2.** There are several other works that have attempted to learn the amount of quantization/precision to use at each layer [66, 67, 68]. However, unlike our work, these works do not directly optimize for FLOPs, latency. We would like to note that our parameterization is closely related to the parameterization of [68].

**Straight Through Estimator (STE).** Note that the training objective for quantization is nondifferentiable. So, in our experiments, we use STE to optimize the objective [69]. This is a standard technique for performing quantization aware training.

 $<sup>{}^{3}</sup>B$  is typically a power of 2

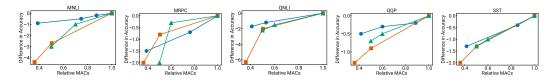


Figure 6: Fine-tuning tradeoffs of BERT on GLUE benchmark.

# **B** Implementation and experimental details

In this section, we provide additional details about the implementation of our technique. We warmstart our pruning procedure with the pre-trained model (*i.e.*,  $f^*$  in Section 3) that is made available to us. In our experiments, we noticed that this speeds up the convergence of our algorithm. For both MobileNetV3 and BERT compression, we rely on simultaneous pruning, low-rank factorization of weights (see Table 1 for details). Here, we parameterize weights  $W_i$  as  $U_i \operatorname{diag}(\beta_i) V_i \operatorname{diag}(\alpha_i)$ ; setting entries of  $\beta_i$  to 0 helps reduce the rank of the weight matrix, and  $\alpha_i$  helps in pruning. We initialize  $U_i, V_i, \beta_i$  by performing SVD on the weight matrices of the pre-trained network. In our experiments, we apply our technique only to the  $1 \times 1$  convolution layers in the network, for which the formulation of our regularizer remains the same as the one described in the preceding text. We anneal our regularization strength  $\lambda$ , increasing it linearly in order to stabilize the training. Finally, we fine-tune the model returned by our pruning algorithm on the training data to improve its performance (this simply involves setting the FLOPs regularization coefficient to 0). During the fine-tuning and pruning phases, we leverage the pre-trained model by adding a distillation loss to the standard crossentropy loss [70]. We perform distillation between the logits of the pre-trained model and the logits of the model being fine-tuned.

#### **B.1 ImageNet Pretraining**

Our algorithm was implemented using TensorFlow 2.0. We use the pre-trained MobileNetV3 (or EfficientNet) models provided in this framework to warm-start our models. We initialize  $U_i$ ,  $\beta_i$ ,  $V_i$  to the SVD of the 1x1 convolution filters, and the entries of  $\alpha_i$  uniformly at random between [0, 0.5]. We use Adam for optimization with its default parameters, and searched over learning rates in the set  $\{10^{-4}, 5 \times 10^{-5}, 10^{-5}\}$ , with cosine decay, which is standard practice. The distillation coefficient was searched among  $\{0.1, 0.25, 0.5, 0.9\}$  and the distillation temperature was searched among  $\{2, 3, 4\}$ . For our ImageNet experiments, We trained our model for 70000 steps, linearly annealing the regularizer for the first 50000 steps. We fine-tuned the obtained model for another 50000 steps. For the transfer learning experiments, we reduced these to 25000 for training and 15000 for fine-tuning. We used a batch size of 2048 for all experiments. Our regularizer coefficient was varied from  $10^{-8}$  to  $10^{-6}$ . This range was determined by looking at the magnitude of the cross-entropy loss and the FLOPs regularizer, and making sure that they are similar. MobileNet pre-training took up around 13 hours.

#### **B.2** Transfer Learning

**BERT.** For the BERT fine-tuning experiments, we start off with a pre-trained BERT model and introduce our parameterization in a similar manner as described above. We use AdamW to optimize, and search over learning rates among  $\{10^{-4}, 5 \times 10^{-5}, 10^{-5}\}$ . Our regularizer coefficient was varied from  $10^{-7}$  to  $5 * 10^{-6}$ . Each fine-tuning run taking between 20 mins - 1 hour.

**EfficientNet, MobileNet.** For EfficientNet and MobileNet experiments, we have similar experimental setup and hyper-parameter search space as MobileNet ImageNet pretraining described in App B.1, with the exception that we do not do any model distillation. We also use RMSProp for EfficientNet with exponential decay as the LR schedule, as this was the optimizer of choice for its pre-training. We train for 25000 steps with the regularizer, and fine-tune for another 25000 steps.

#### **B.3** Quantization

We train a CNN with four convolution layers, with [64,128,256,128] filters and kernel size of 3 with stride being 1 for each layer. We additionally have batch-norm layers after each conv layer. We search for learning rate over {1e-4, 5e-4, 1e-3, 5e-3} for the baseline and our model, and regularizer coefficient over {1e-9, 3e-9, 5e-9, 7e-9, 1e-8}. We train for 100 epochs with a batch size of 512 on a single V100 GPU, and use Adam with CosineDecay for the learning rate.

#### **B.4** Latency Tables

As mentioned in the main paper, the actual on-device latencies are calculated on Pixel6 for our latency experiments. We populated the latency lookup-table T specified in Section 3.3 by profiling the corresponding  $1 \times 1$  convolution/matrix-vector multiplication latency, on the device. Note that the convolution operation is much better optimized than matrix multiplication operation on the Pixel6 kernel. Hence, for our latency experiments on MobileNet, the latency table was populated by profiling the  $1 \times 1$  convolution operations.

A 1x1 convolution operation is identified by input dimension, input channels and the number of filters (output channels). Strides can also be different but all 1x1 convolutions in the MobileNet architecture have stride 1. In the MobileNet architecture we encounter feature maps with input dimensions  $in_{dim} \in I = \{1, 7, 14, 28, 56, 112, 224\}$ . Moreover, the input (in<sub>c</sub>) and output channels (out<sub>c</sub>) are constrained by in<sub>c</sub>, out<sub>c</sub>  $\in D = \{d | \forall d \in \mathbb{N} \text{ and } d < 1281\}$ . Hence we construct the table T, each member of which can be accessed via  $T(in_{dim}, in_c, out_c)$ . Note that profiling  $T(in_{dim}, in_c, out_c)$ . for every possible value of  $(in_{dim}, in_c, out_c) \in I \times D \times D$  is expensive. We must therefore pick certain tuples (in<sub>c</sub>, out<sub>c</sub>) for each  $in_{dim} \in I$  for which we calculate actual on-device latencies. The rest of the table is populated using linear interpolation. We pick these tuples such that they cover the  $1 \times 1$ convolutions that are encountered in the MobileNet Architecture. For  $in_{dim} = \alpha$ , let  $\beta$  denote the maximum possible value of in<sub>c</sub>, and  $\gamma$  denote the maximum possible value of out<sub>c</sub> in MobileNet. We construct set  $P_{in}$  which denotes values that are likely to be encountered by the regularizer for in<sub>c</sub> and similarly  $P_{out}$  for out<sub>c</sub>. Finally, the actual on-device latencies are calculated for  $T(\alpha, P_{in} \times P_{out})$ . Construction of  $P_{in}$  and  $P_{out}$  is done by choosing an appropriate  $\theta$  and adding all values in the range  $(\beta - \theta, \beta]$  to  $P_{in}$ , and  $(\gamma - \theta, \gamma]$  to  $P_{out}$ . Also, from the remaining ranges i.e.  $(0, \beta - \theta]$  and  $(0, \gamma - \theta]$ points are sampled exponentially by choosing the midpoint of the range every time and changing the lower limit of the range to the midpoint for certain iterations.

The experimental setting and hyper-parameter configurations we use for latency table experiments is same as the one for FLOPs experiments (see Section B.1).

# C Additional Experimental Results

#### C.1 Pretraining ResNet on ImageNet

In this section, we present additional experimental results to demonstrate the generality of our approach. We compress the ResNet architecture for ImageNet classification, using our method. In particular, we compress the  $1 \times 1$  convolutions using pruning and low-rank factorization. We compare our method against HALP [71] and PAS [72], two state of the art methods for architecture search and compression for ResNet. Our method compresses ResNet-101 to a model with similar FLOPs as ResNet-50, while simultaneously achieving better performance than the baseline ResNet-50. Furthremore, our technique outperforms SOTA methods for the same number of FLOPs, as seen in Fig 7. We use the same hyper-parameters as those described in Sec B.1, but we vary the FLOP regularizer coefficient between [1e-10, 1e-9] since ResNet models have a higher number of FLOPs.

#### C.2 Ablation Studies

**Effect of sparsity norm.** In section 3 we provided small scale experiments to justify our design choices of using projected-Adam and  $\frac{\ell_1}{\ell_2}$  norm. In this section we perform large-scale ablation studies on MobileNetV3 for ImageNet training. The results from this experiment are presented in Figure 8. Without projected-Adam, we notice that the optimization algorithm doesn't converge to sparse solutions. Consequently, the resulting models do not have large reduction in MACs. The accuracy of

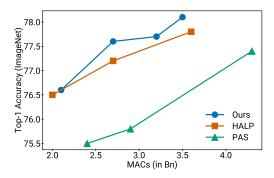


Figure 7: **Pruning ResNet on ImageNet**: We compare against HALP and PAS, two recent SOTA techniques to prune ResNet-50, and achieve better performance over different FLOP regimes.

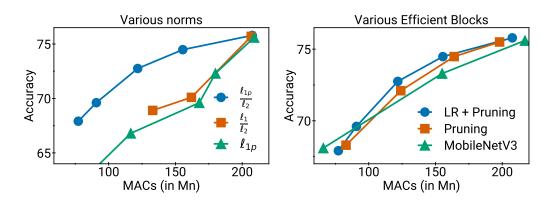


Figure 8: Ablation studies on ImageNet: We compare using  $\ell_1$  and  $\frac{\ell_1}{\ell_2}$  norms in our regularizer, with subscript p indicating that projected-Adam was used for optimization. We also experiment with combining low-rank (LR) factorization with channel pruning.

these models also takes a big hit. On the other hand, using  $\ell_1$  norm based FLOPs regularizer with projected-Adam suffers from the scaling issue described in Sec 3.2. This leads to a large fraction of channels being pruned for some blocks, producing a model with deteriorated accuracy. Our method has 2-4% better accuracy in the high and mid FLOPs regimes than these alternatives.

**Comparing different building blocks.** In Table 1, we described ways to integrate various building blocks into our framework. In Figure 8, we demonstrate the accuracy *vs* inference time trade-offs of using two of these building blocks in our framework, namely Pruning and Pruning+Low-rank Factorization. We find that the extra flexibility provided by the Low-Rank Factorization leads to models with fewer MACs for the same accuracy, and the difference is even more pronounced for smaller models. We note that channel pruning alone can give us 10% reduction in MACs over the MobileNetV3 family at the same accuracy level. In particular, at 73.4% accuracy, our model has 136Mn MACs compared to 155Mn MACs of the MobileNetV3 family model. Similarly, at 75.5% accuracy, our model has 198Mn MACs comopared to 216Mn MACs of MobileNetV3 family model. Adding Low-Rank structure introduces another 5% reduction in MACs over the gains from channel pruning, with no loss in accuracy. This also shows the effectiveness of our algorithm across multiple building blocks. Combining other efficient blocks such as block structured sparsity, quantization is a direction for future investigation.

#### **D** Combination of building blocks

Table 2 presents the parameterization of weight matrices that lets us search over multiple building blocks simultaneously.

Efficient Building Block	Parameterization of $W_i$	FLOPs ( <i>i</i> <sup>th</sup> layer)	<b>Regularizer (FLOPs surrogate)</b> ( <i>i</i> <sup>th</sup> layer)
Pruning + Unstructured Sparsity	$(W_i \odot \beta_i) \times \text{diag}(\alpha_i),$ $\odot$ is the elementwise multiplication operator	$\ \operatorname{Vec}(\beta_i \times \operatorname{diag}(\alpha_i))\ _0$	$\frac{\sqrt{d_i d_{i+1}} \  \operatorname{Vec}(\beta_i \times \operatorname{diag}(\alpha_i)) \ _{1p}}{\  \operatorname{Vec}(\beta_i \times \operatorname{diag}(\alpha_i)) \ _2}$
Pruning + Quantization (1, 2, 4 bit quantization)	$ \begin{pmatrix} W_{i,1} + \alpha_{i,2}(\Delta_{i,2} + \alpha_{i,4}(\Delta_{i,4})) \\ \times \operatorname{diag}(\beta_i), \end{pmatrix} $	$ \begin{pmatrix} \ (1-\alpha_{i,2})\ _{0} + \\ 2\ \alpha_{i,2}(1-\alpha_{i,4})\ _{0} + \\ 4\ \alpha_{i,2}\alpha_{i,4}\ _{0} \end{pmatrix} \times \ \beta_{i}\ _{0}\ \beta_{i+1}\ _{0} $	$ \begin{pmatrix} \frac{\ell_1}{\ell_2} \text{ norm of} \\ \text{the vector } [(1 - \alpha_{i,2}), \\ 2\alpha_{i,2}(1 - \alpha_{i,4}), 4\alpha_{i,2}\alpha_{i,4}] \end{pmatrix} \\ \times \frac{\sqrt{d_i} \ \beta_i\ _p}{\ \beta_i\ _2} \frac{\sqrt{d_{i+1}} \ \beta_{i+1}\ _{1p}}{\ \beta_{i+1}\ _2} $

Table 2: Table describing regularizers used by our technique for various efficient building blocks.

# **E** Limitations and Broader Impact

One limitation of our work is that we only study popular building blocks such as sparsity, pruning, low-rank factorization and quantization. Extending our work to more building blocks such as block sparsity and other forms of structured sparsity is an interesting future direction. Another limitation, which is related to the implementation of our technique, is the need to manually implement the FLOPs regularizer for various architectures. An automated solution that takes in any architecture and computes the FLOPs regularizer would make our framework easy to use.

In terms of broader impact, we believe our technique can be used to find more efficient architectures for large language models such as GPT. This can help democratize these models, and also reduce their carbon footprint.